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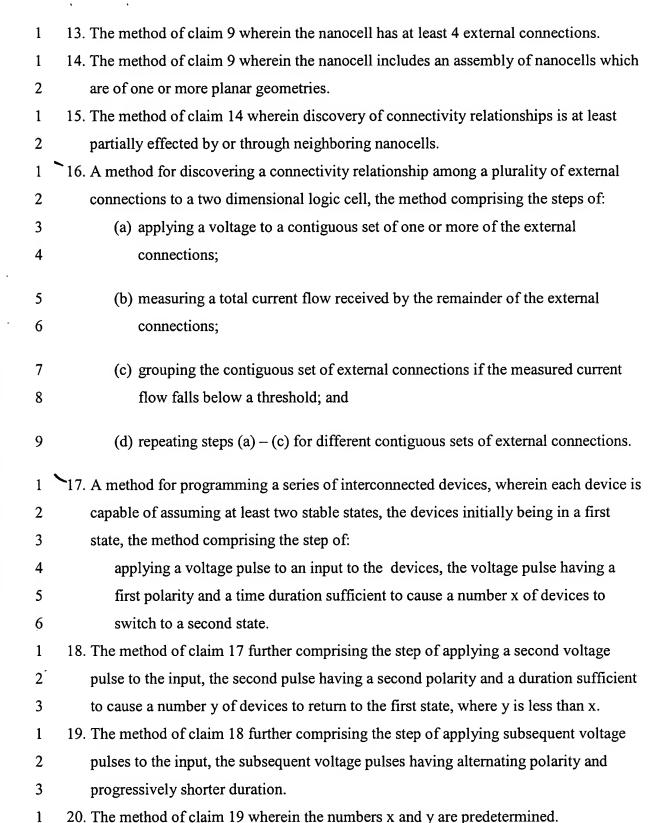
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I claim:

- 1 1. A method for discovering a connectivity relationship among a plurality of external connections to a two dimensional logic cell, the method comprising the steps of:
 - (a) for all contiguous sets of one or more of the external connections, applying a voltage to each contiguous set and measuring a total current flow received by the remainder of the external connections;
- 6 (b) examining a current flow measurement corresponding to a contiguous set of the external connections;
- 8 (c) grouping the contiguous set of external connections if the measured current 9 flow falls below a threshold; and
- 10 (d) repeating steps (b)-(c) for different contiguous sets of external connections.
- The method of claim 1 wherein each previously grouped set of external connections
 is treated as a single external connection.
- 3. The method of claim 1 further comprising the step of using the connection groupings
 to discover a logical relationship among the external connections.
- 4. The method of claim 3 wherein the connection groupings are used to generate an
 ordered binary decision diagram (OBDD).
- 5. The method of claim 4 wherein the connection groupings comprise a set of variables
 and orderings on those variables that are used to generate the OBDD.
- 1 6. The method of claim 1 wherein the current flow threshold is predetermined.
- 7. The method of claim 1 wherein the current flow threshold is dynamically determined.
- 1 8. The method of claim 1 wherein the logic cell is a nanocell.
- 1 9. The method of claim 8 wherein the nanocell is a regular polygon.
- 1 10. The method of claim 9 wherein the regular polygonal nanocell is further
- 2 characterized by one or more external connections on one or more sides of the
- 3 polygon.
- 1 11. The method of claim 9 wherein each side of the polygonal nanocell has at least one
- 2 external connection.
- 1 12. The method of claim 9 wherein the nanocell has at least 20 external connections.

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21. The method of claim 19 wherein the numbers x and y are dynamically determined.

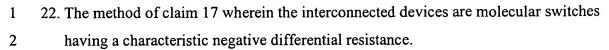
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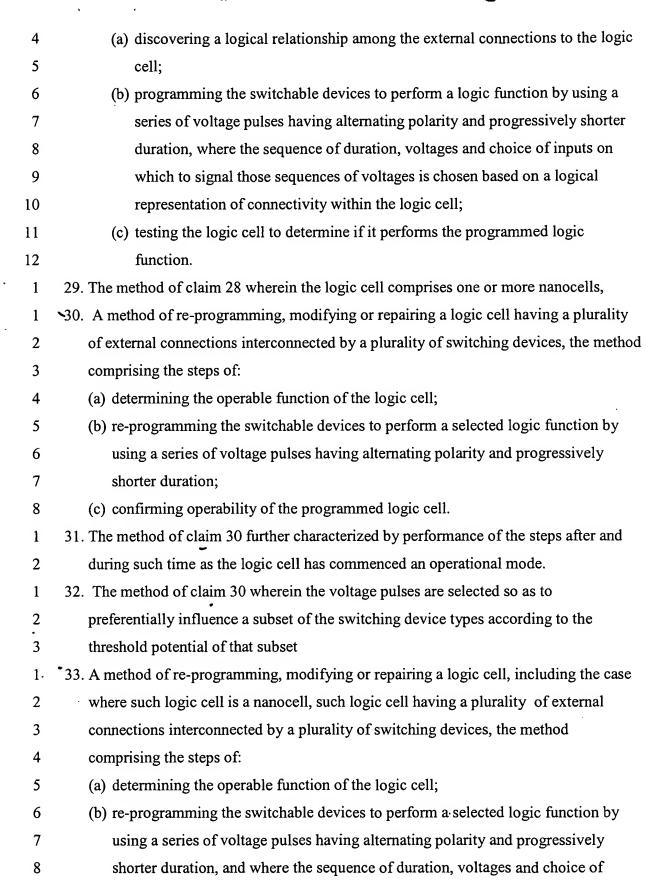
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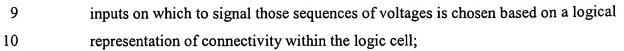
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- 23. The method of claim 17 wherein the logic cell includes switching devices of different
 switching potentials.
- 24. The method of claim 17 further including the step of devices assuming a known state
 at some time subsequent to the application of the first pulse.
- 25. The method of claim 17 wherein the interconnected device are molecular switches
 within nanocells, and wherein logic cell programming is at least partially effected by
 or through neighboring nanocells.
- applying a voltage pulse to an input to the devices, the voltage pulse having a first polarity and a time duration sufficient to cause a number x of devices to switch to a second state.
- 27. A method for programming a logic cell having a plurality of external connections
 interconnected by a plurality of switching devices, the method comprising the steps
 of:
 - (a) discovering a logical relationship among the external connections to the logic cell;
 - (b) programming the switchable devices to perform a logic function by using a series of voltage pulses having alternating polarity and progressively shorter duration;
- 9 (c) testing the logic cell to determine if it performs the programmed logic function;
- 11 (d) repeating steps (a)-(c) as necessary to ensure the logic cell performs the 12 programmed logic function.
- 28. A method for programming a logic cell having a plurality of external connections
 interconnected by a plurality of switching devices, the method comprising the steps
 of:





- (c) confirming operability of the programmed logic cell.
- 34. The method of claim 33 further characterized by performance of the steps after and
 during such time as the logic cell has commenced an operational mode.
- 35. The method of claim 33 wherein the voltage pulses are selected so as to
 preferentially influence a subset of the switching device types according to the
 threshold potential of that subset.
- 1 γ 36. A device containing at least one logic cell programmed by the method of claim γb^{γ}
- 1 | 37. A device containing at least one logic cell programmed by the method of claim 17.
- 1 38. A device containing at least one logic cell programmed by the method of claim 26.
- 1 _ 39. A device containing at least one logic cell programmed by the method of claim 27.
- 1 40. A device containing at least one logic cell programmed by the method of claim 28.
- 1 41. A device containing at least one logic cell programmed by the method of claim 29
- 1 42. A device containing at least one logic cell programmed by the method of claim 30.
- 1 / 43. A device containing at least one logic cell programmed by the method of claim 33.